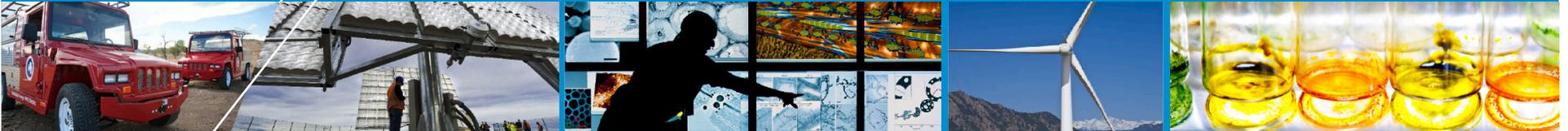


Overview of IEC Testing for PID



Peter Hacke

National Renewable Energy Laboratory (NREL)

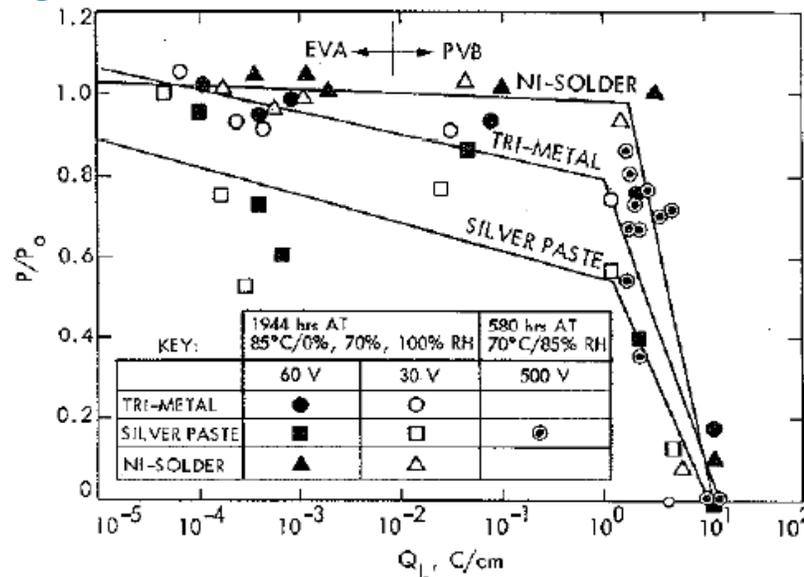
Overview

- **Introduction of mechanisms**
- **IEC 62804 – overview/history of PID test method**
- **Present status of test types**
 - Chamber test
 - Foil test
- **Future of IEC testing for system voltage stress**
 - Basic level testing (such as for qualification testing)
 - Climate-specific, lifetime predictions
- **Understanding of stress factor interactions**
 - Multi factor cyclic/combined stress testing

Introduction/background

- Mon, Ross/JPL 1970s and 1980s

Degradation with ionic current coulombs transferred (c-Si, a-Si)

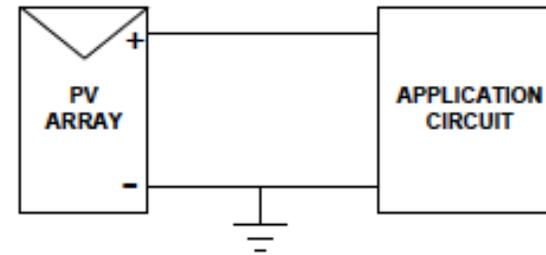
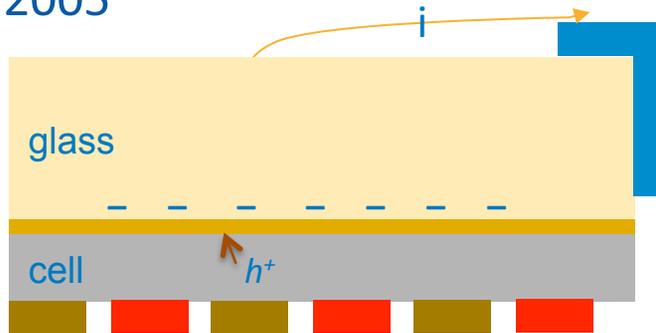


JPL- Mon, Ross (1985)

- Wohlgemuth/BP Solar (2000) showed TCO corrosion
- Osterwald/NREL (2003) showed corrosion occurs in the $\text{SnO}_2:\text{F}$ transparent conductor layers in a-Si and CdTe modules; mitigated by:
 - Lowering humidity
 - Reduction of voltage potential between the frame and the active layer
 - More resistive packaging: changing from soda lime to borosilicate glass,
 - Moving the frame from the glass edge to adhesive bonding on the module rear

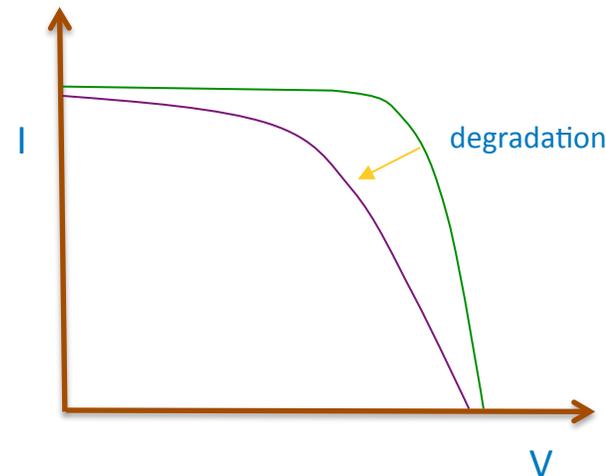
Introduction/background

SunPower reports 'surface polarization' in n-base Si modules (field and test) in 2005



Swanson et al, Asian PVSEC (2005)

- Positive bias string leads to leakage current through glass to ground, leaving negative charge on cell surface, degrading effectiveness of the n⁺ front surface field of the n⁺/n structure
- Minority carriers (holes) recombine at front surface, leading to degraded cell performance
- SunPower *also* reports system voltage degradation in p-base Si modules (2005)
- Evergreen – field degradation (2008), SOLON – field degradation and testing (2010), NREL – testing(2010)

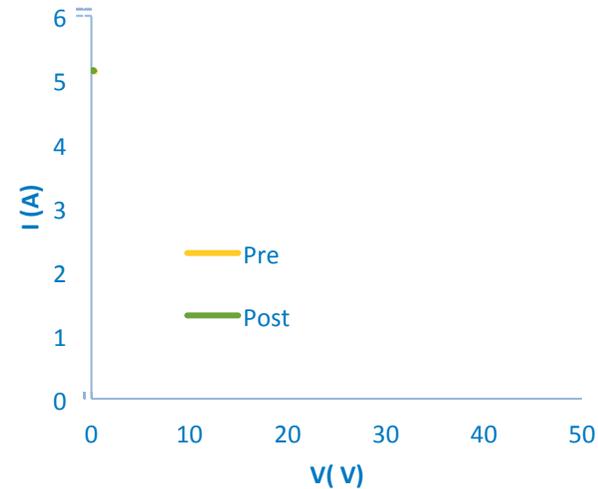
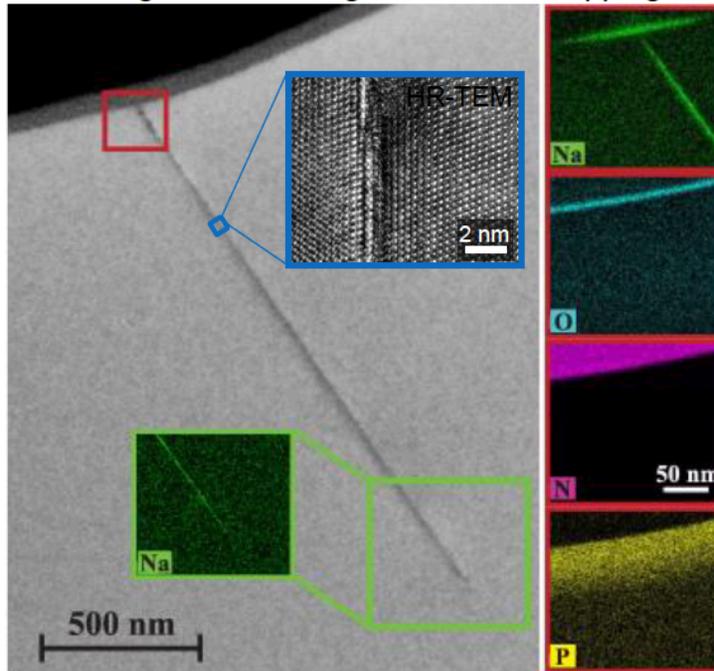


Introduction: Physical nature of PID n+/p Si cells

Negative system voltage strings

1. Positive Na ions electromotively attracted through encapsulant to silicon cell
2. Na diffusion to junction through stacking faults, $f(T, |Na|)$

TEM image of a stacking fault + EDX mapping:



V. Naumann (*Sol.Mat.* 2014)

- PID-shunt = 2D crystal defect (“stacking fault”) in Si, decorated with Na ^[1]

Stacking faults

- Associated with the crystal growth
- Can be created and annihilated with high temperature diffusions and oxidation

IEC 62804 TS– Overview of scope

- Screening test to evaluate c-Si PV modules to the effects high voltage stress including potential-induced degradation (PID) and polarization
- Glass surfaces, silicon cells having passivating dielectric layers, for degradation mechanisms involving mobile ions
- Measures short term effects
 - Does not deal with encapsulation failure that in turn leads to rapid moisture ingress and electrochemical corrosion.

IEC 62804 – Brief history

- Concept for a system voltage durability test proposed Fall 2010 WG2 meeting
 - Contained damp heat with voltage bias stress test
 - WG2 membership needed time to study the matter
- New work item proposal published Dec. 2011
 - “System voltage durability test for crystalline silicon modules - Qualification and type approval”
- Two votes at WG2 meetings moved the document to a test method; reasons held by some include:
 - Not enough understanding to standardize pass/fail criteria
 - Module makers needed to be convinced it was necessary
 - Better to include pass/fail criteria in IEC 61215
- Fall 2013/Spring 2014:
 - Added Al foil test parallel to the environmental chamber test
 - Simple test, but not able to evaluate module designs with frame/mounting-based mitigation
 - Changed to a test method (IEC technical specification)
- IEC 62804 TS: Test methods for detection of potential-induced degradation of crystalline silicon photovoltaic (PV) modules
 - Draft approved by national committee voting on 2015-01-09
 - Final submission, adjusting language and other minor items, *very soon*

IEC 62804 – Brief history

- Concept for a system voltage durability test proposed Fall 2010 WG2 meeting
 - Contained damp heat with voltage bias stress test
 - WG2 membership needed time to study the matter
- New work item proposal published Dec. 2011
 - “System voltage durability test for crystalline silicon modules - Qualification and type approval”
- **Qualification test**

 - Two votes at WG2 meetings showed the document to a test method; reasons held by some include:
 - Not enough understanding to standardize pass/fail criteria
 - Module producers needed to be convinced it was necessary
 - Better to include pass/fail criteria in IEC 61215
- Fall 2013/Spring 2014:
 - Added Al foil test parallel to the environmental chamber test
 - Simple test, but not able to evaluate module designs with frame/mounting-based mitigation
 - Changed to a test method (IEC technical specification)
- IEC 62804 TS: Test methods for detection of potential-induced degradation of crystalline silicon photovoltaic (PV) modules
 - Draft approved by national committee voting on 2015-01-09
 - Final submission, adjusting language and other minor items, *very soon*

Damp heat and foil methods – setup

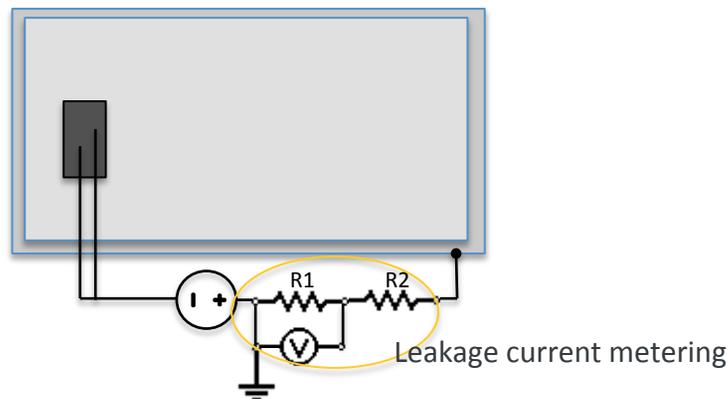


Damp Heat

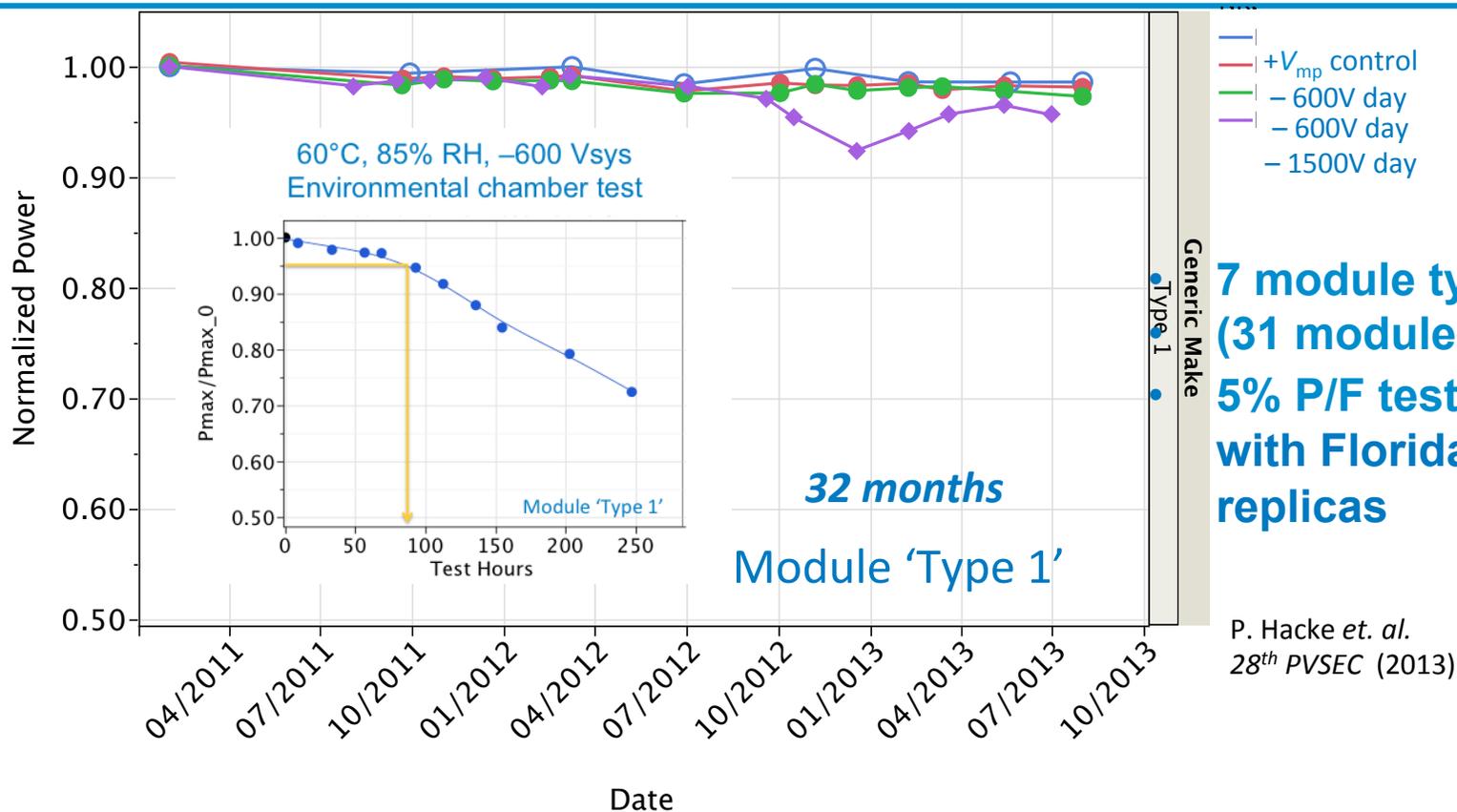


Foil

Bagdahn, Fraunhofer CSP
PV Japan, 5-7 Oct 2012



Origin of damp heat stress test



**7 module types
(31 modules)
5% P/F test works so far
with Florida-fielded
replicas**

P. Hacke *et. al.*
28th PVSEC (2013)

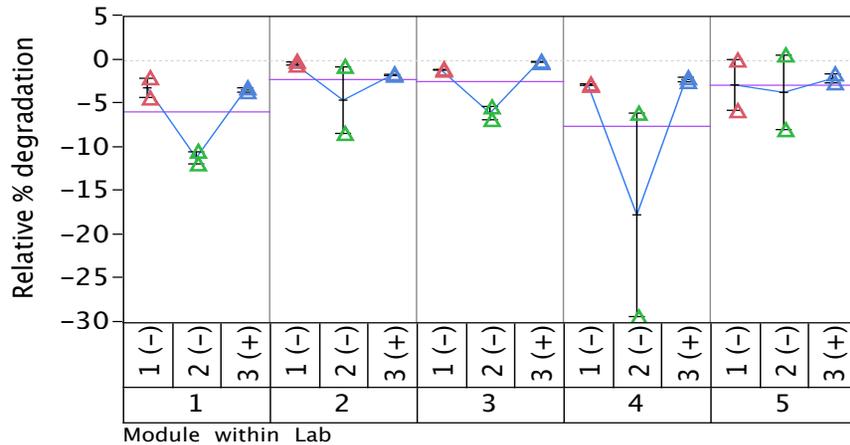
Take note: For reproducibility, not qual testing “test method IEC 62804 TS” changes:

- Startup sequence to eliminate excess humidity on module
- Tolerances for relative humidity tightened

Results is a weakened 60°C 85% RH stress test.

Recalibration of relationship required with new startup sequence

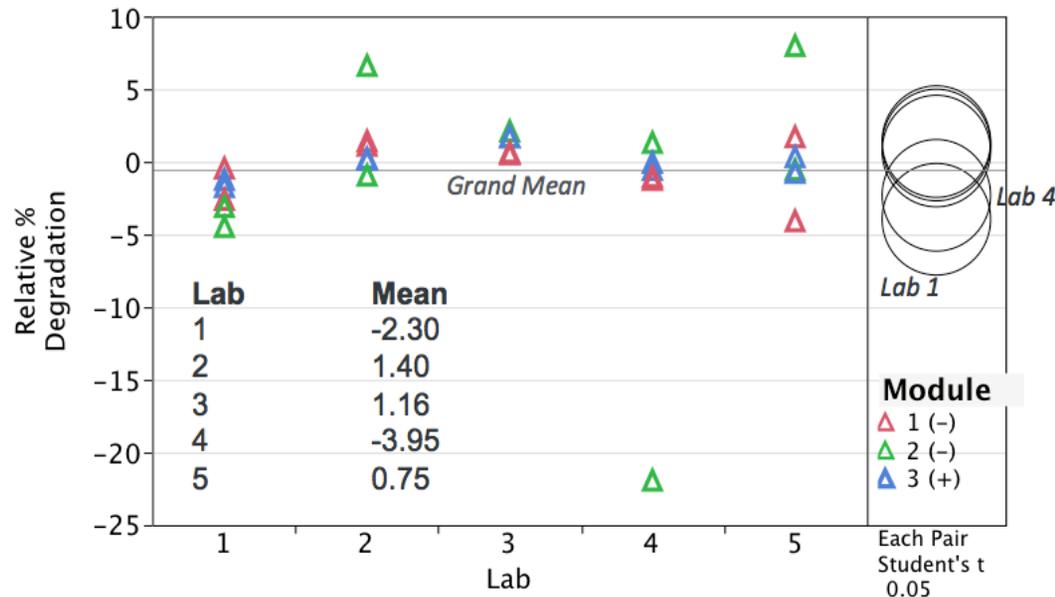
Reproducibility/repeatability– damp heat stress test



Older (CD) profile: 60°C/85% RH, Vsys

- 3 module types
- 2 replicas/polarity
- 5 labs

NREL
 PI-Berlin
 Fraunhofer ISE
 TÜV Rheinland
 Fraunhofer CSP



- Subtracting median degradation for each module type
- Failed to show a statistical significance in difference between labs.
- Data shows sufficient reproducibility for qualification test

Move to test method:

Startup sequence changed to mitigate non-equilibrium excess moisture on modules during startup

- Expected improved reproducibility
- Weakens test significantly

P. Hacke et al, JPV (2015)

Conditions for damp heat stress test

These severities represent the minimal stress levels for detection of PID.

- Module temperature: $60\text{ }^{\circ}\text{C} \pm 2\text{ }^{\circ}\text{C}$;
- Chamber relative humidity: $85\% \pm 3\%$ relative humidity;
- Dwell: 96 h
- Voltage: module rated system voltage and polarities.

Note : Suggested common temperatures to use for the detection of PID for further acceleration: $65\text{ }^{\circ}\text{C}$ and $85\text{ }^{\circ}\text{C}$.

Origin of foil test

- Joint press release of:
 - Fraunhofer ISE,
 - Photovoltaic Institute Berlin
 - TÜV Rheinland,
 - VDE,
 - Q-Cells,
 - Schott Solar
 - Solon

“First Test Conditions for Potential Induced Degradation (PID) of Solar Modules Developed”, September 5, 2011

- Too early to establish a general industry guideline or an international standard.
- An easy method avoiding any need of expensive equipment to check solar modules of their PID reliability.

Koch et al, 26th PVSEC (2011)

Conditions for foil test

These severities represent the minimal stress levels for detection of PID.

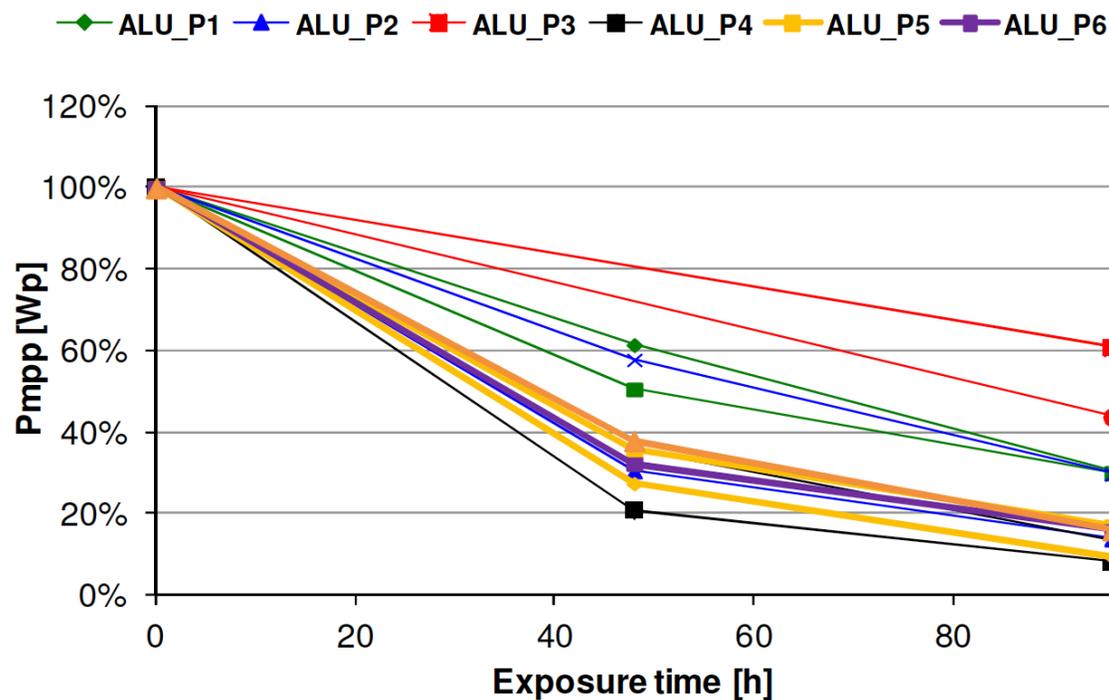
- Module temperature: 25 °C ± 1 °C
- Relative humidity: less than 60 %;
- Test duration: 168 h
- Voltage: module rated system voltage and polarities.

Note : Suggested common temperatures to use for the detection of PID with further acceleration: 50 °C and 60 °C.

Reproducibility/Repeatability – foil test

- PID test results from six test labs testing to the test procedure for 25°C/Al/-1000V/96
 - 1 'sensitive' module type
 - 2 replicas/lab

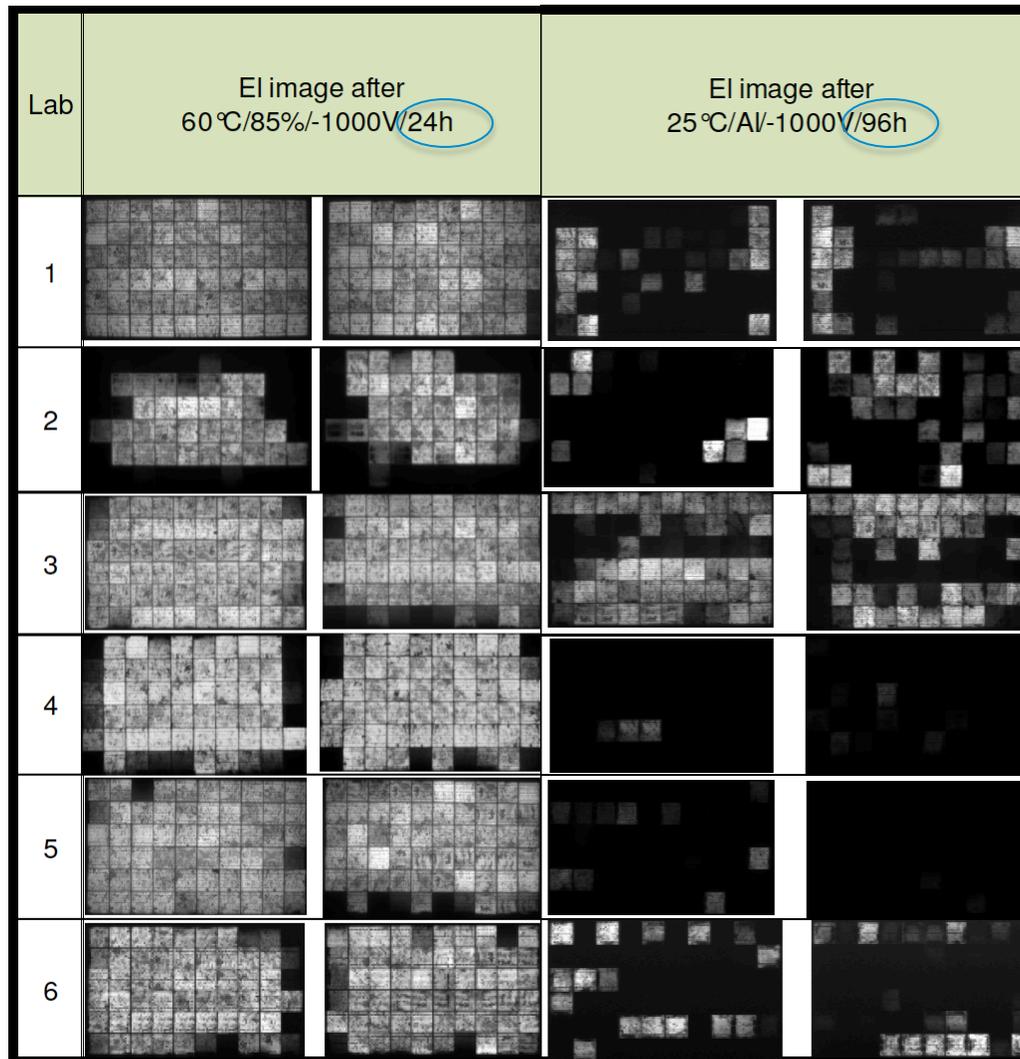
PI Berlin
 NREL
 Fraunhofer ISE
 TÜV Rheinland
 SGS
 UL
 SOLON



Partner	PID in % after 25°C/Al/1000V/96 h	
	Module 1	Module 2
1	69	70
2	86	70
3	39	56
4	92	87
5	83	91
6	84	84

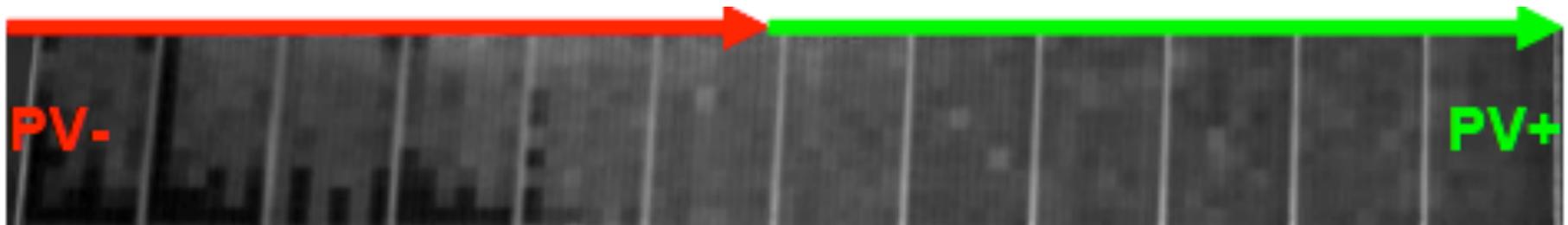
Berghold et al, 28th PVSEC (2013)

EL images of chamber & foil tested modules

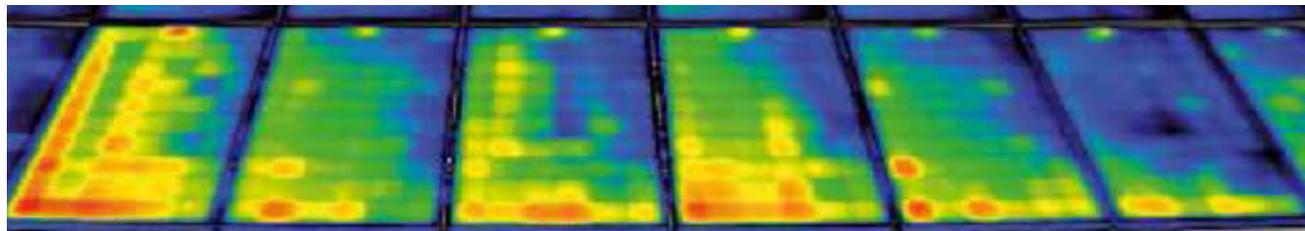


Berghold et al, 28th PVSEC (2013)

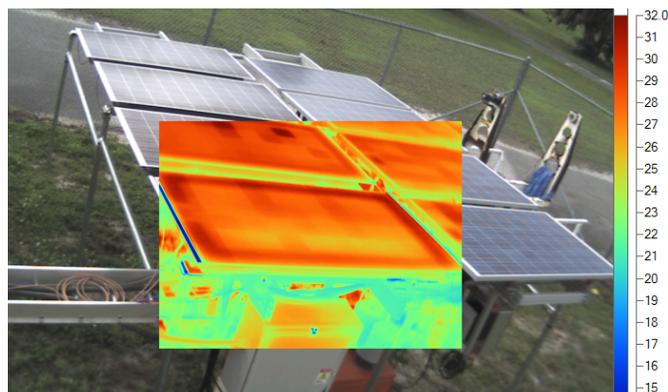
Imaging of PID c-Si modules in the field



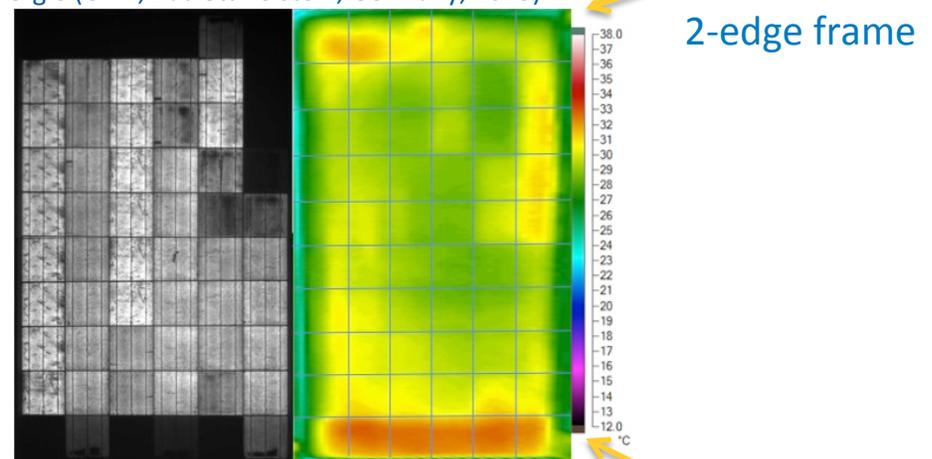
S. Pingel, O. Frank, M. Winkler, S. Daryan, T. Geipel, H. Hoehne and J. Berghold SOLON SE, Presented at 35th IEEE PVSC, 2010



B. Weinreich, Proc. 28th Symposium Photovoltaische Solarenergie (OTTI, Bad Staffelstein, Germany, 2013)



4-Edge frame, -1000 V, 3 years, Florida Schneller/Hacke



2-Edge frame (top/bottom), -1000 V, 3 years, Florida Schneller/Hacke

Modules typically are more stressed at the frame edges

Future of IEC testing for system voltage stress

- **Test method development**
 - *c-Si exists in IEC 62804 TS ed. 1*
- **Qualification testing (basic level)**
- **Climate-specific**
- **Lifetime prediction (higher stress levels Combined/cyclic stresses)**

Integration needed into some of the above:

Heterostructures

Thin film

Understanding of new technologies

Understanding of interactions

factors: light, humidity ingress, stress: multi-mechanism...

mechanisms: delamination, corrosion...

Test method/ Qualification testing (basic level)

- **Experience required to agree upon qualification test level determination for PID**
 - Accelerated test/outdoor comparisons in various environments
 - Modeling
- **Inclusion of thin film; not just new materials, but new mechanisms**
 - Philosophical question about what levels of stress will be acceptable
 - Na interactions with active/absorber layer degrading efficiency
 - Na migration, humidity →TCO corrosion
 - Columbic relationships may be possible with TF (P. Lechner, T. Weber)



P. Lechner, 2013 PVMRW

Understanding of interactions

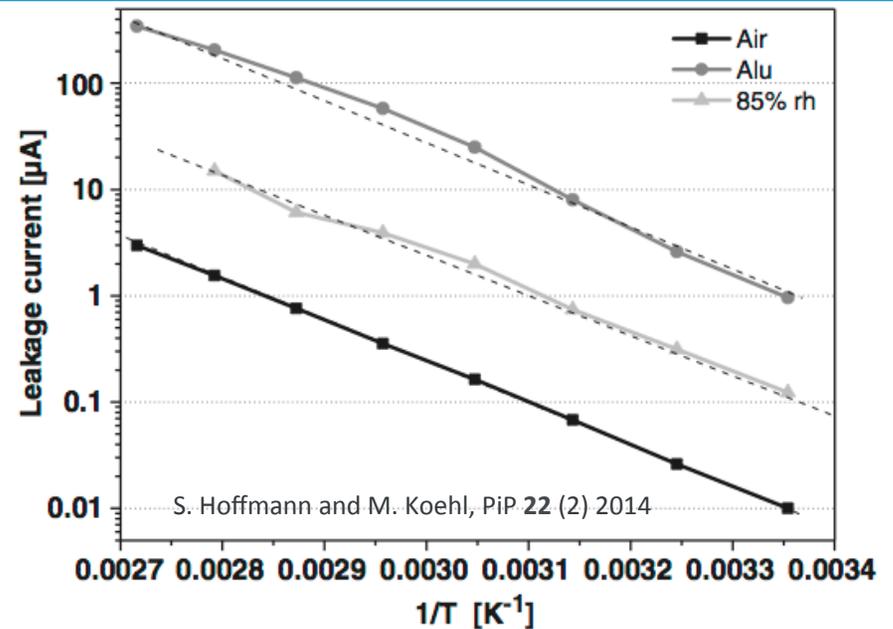
Factors affecting degradation:

- Temperature
- Relative humidity
- Voltage
- PID Stress history/ effective stress
- Light
- Thermal-activated recovery
- Charge build-up over SiN
- Encapsulant resistivity
- Soiling
- Mounting
- ...

Factors for degradation: T

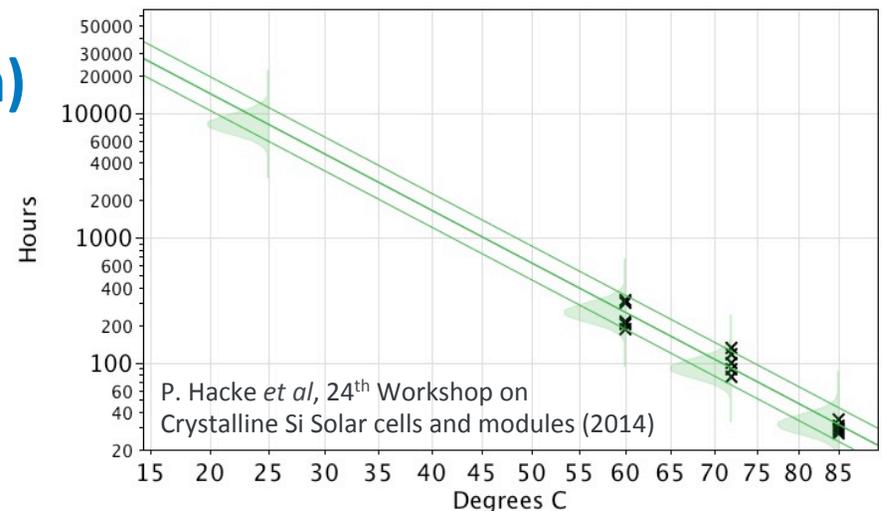
- Leakage current dependency

- Activation energy same; independent of contacting scheme
75kJ/mol; 0.78 eV
 - Low RH (room)
 - Aluminum Foil on Surface
 - 85% RH

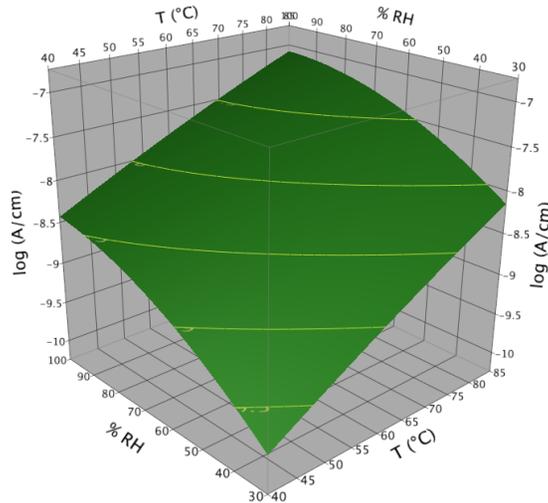


- PID rate (to 1% P_{max} degradation)

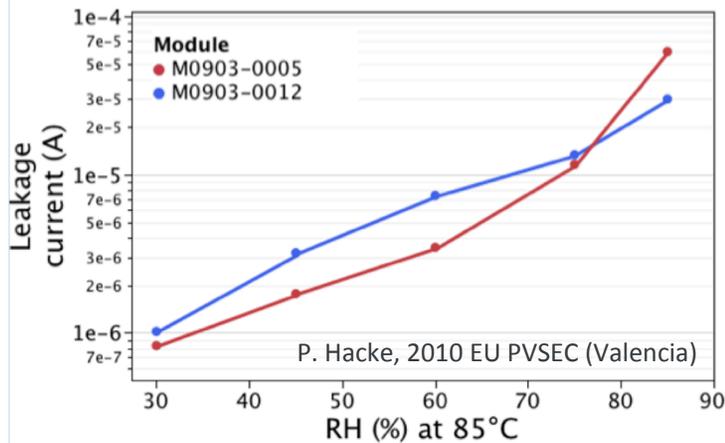
- 82 kJ/mol; 0.85 eV



Factors for degradation: Relative humidity

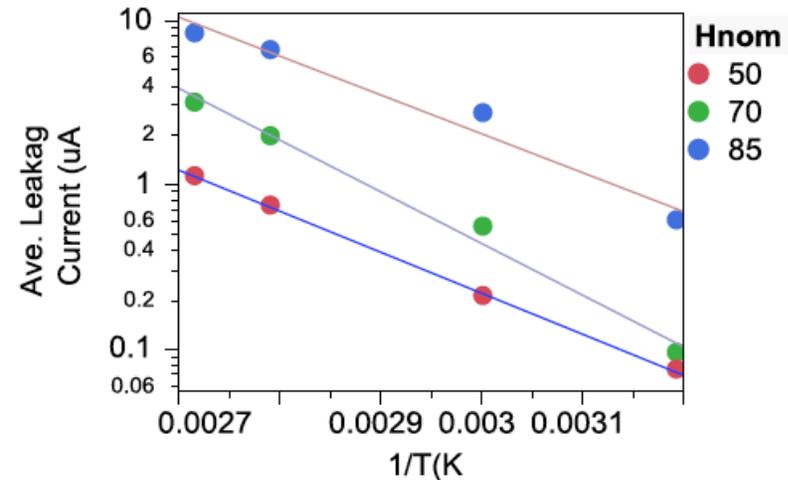


Adapted from G. Mon et al, (JPL), 18th IEEE PVSC (1985)



P. Hacke, 2010 EU PVSEC (Valencia)

Bivariate Fit of Ave. Leakage Current (uA) By 1/T(K) Voltage Applied=-600



Kent Whitfield, 2014 NREL PV Module reliability workshop

$$LC = A \cdot e^{n \cdot RH} \cdot e^{\frac{-Ea}{k \cdot T}} \cdot f(V) \text{ and } f(V) \propto V$$

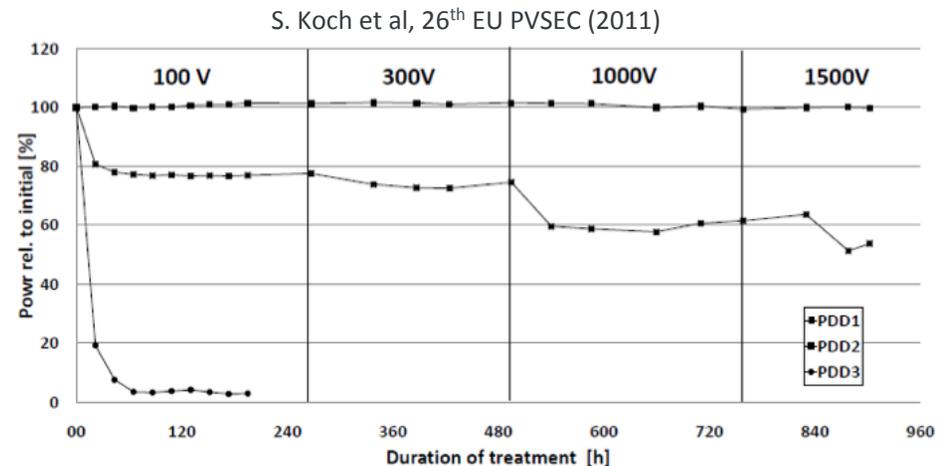
$$LC(\mu A) = 2200(\mu A / V) \cdot V_{sys}(V) / 2 \cdot e^{0.06 / \%RH_{module}(\%)} \cdot e^{\frac{-0.5eV}{k \cdot T_{module}}}$$

- Exponential model fit

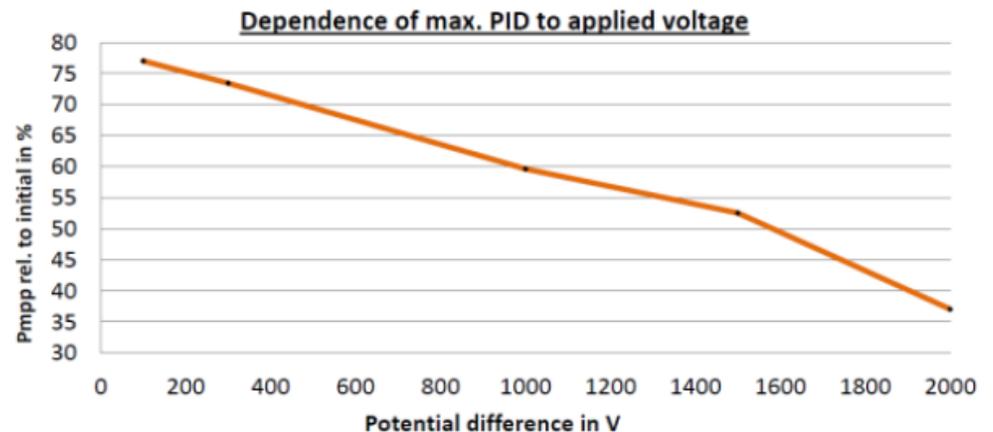
- Leakage current can be reasonably described considering RH and T
 - Has been iterated over various climates assuming you can determine module T and atmospheric RH → module RH

Factors for degradation: Voltage

- Leakage current generally seen to be linear with voltage both in chambers and outdoors ($V=IR$)
- Maximum stabilized degradation has been linked with applied voltage

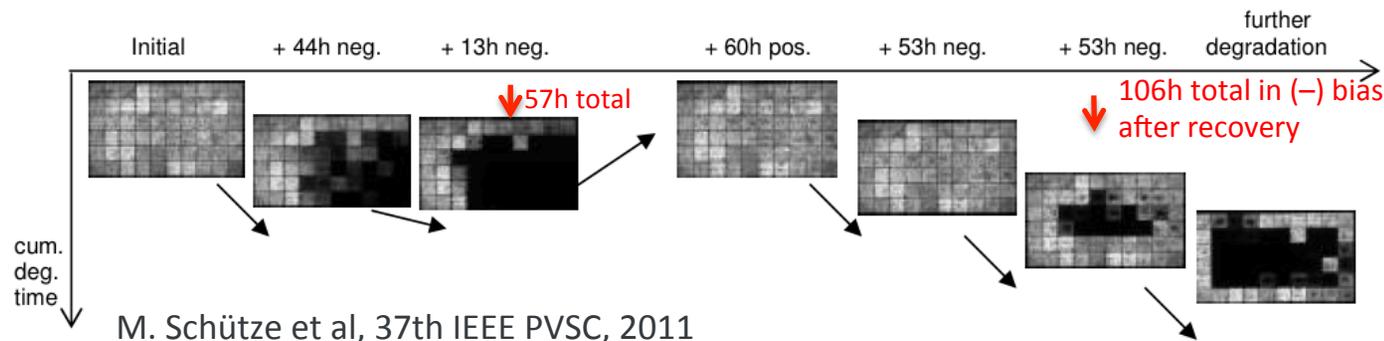
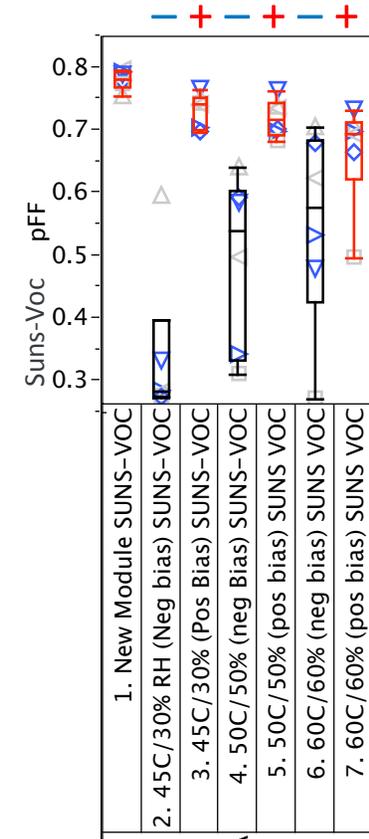
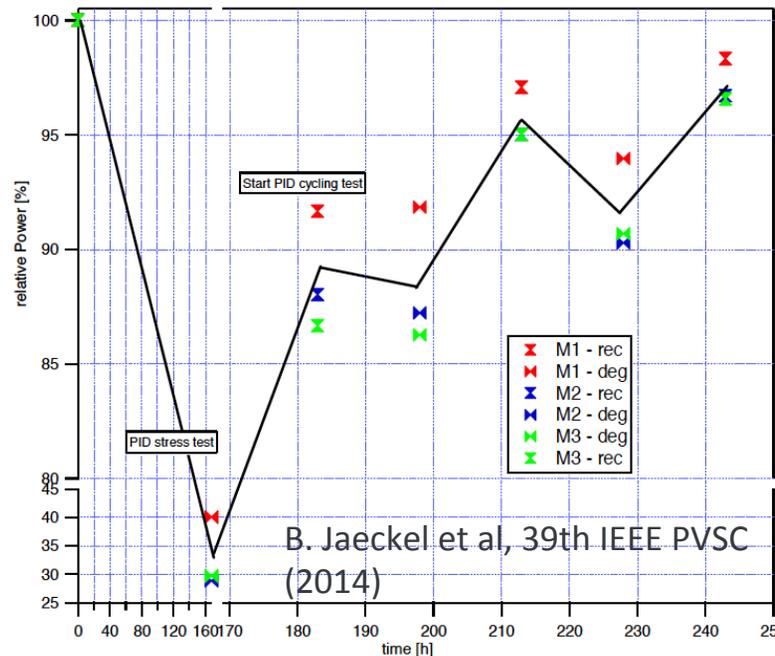
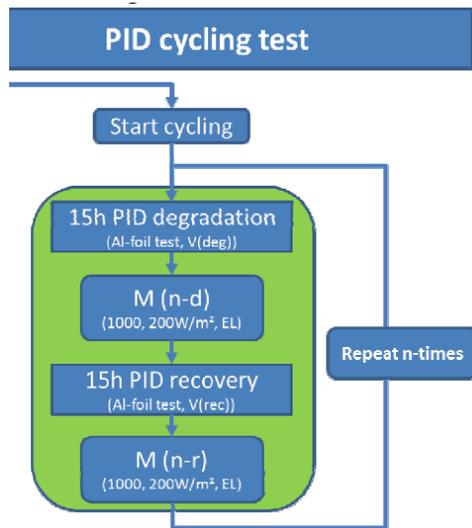


S. Koch et al, 27th EU PVSEC (2012)



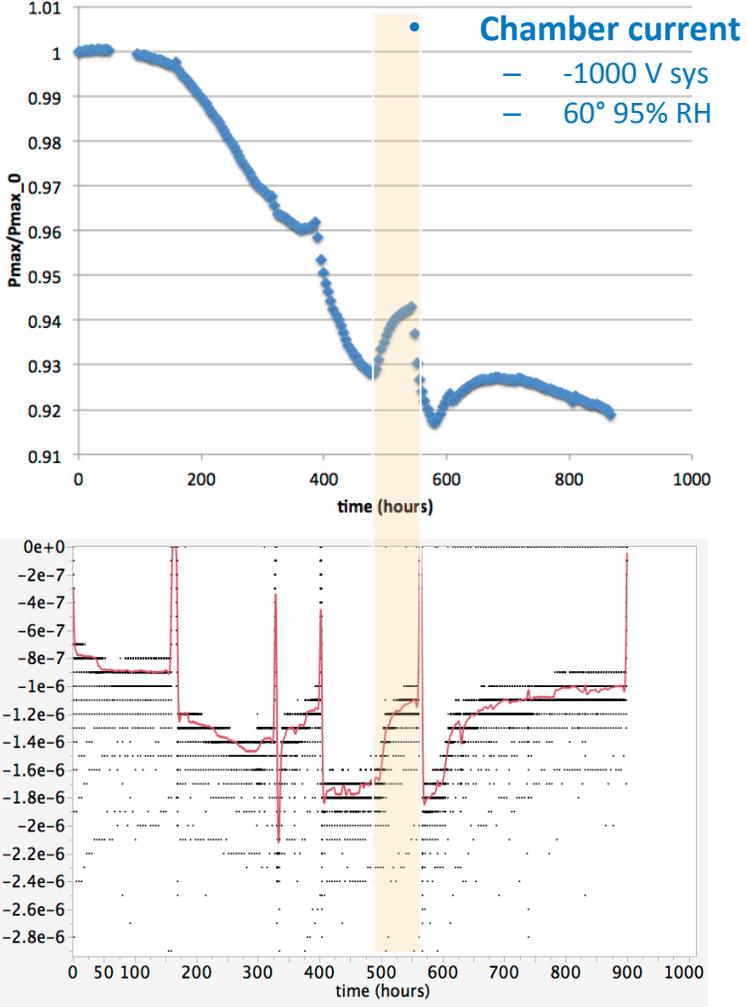
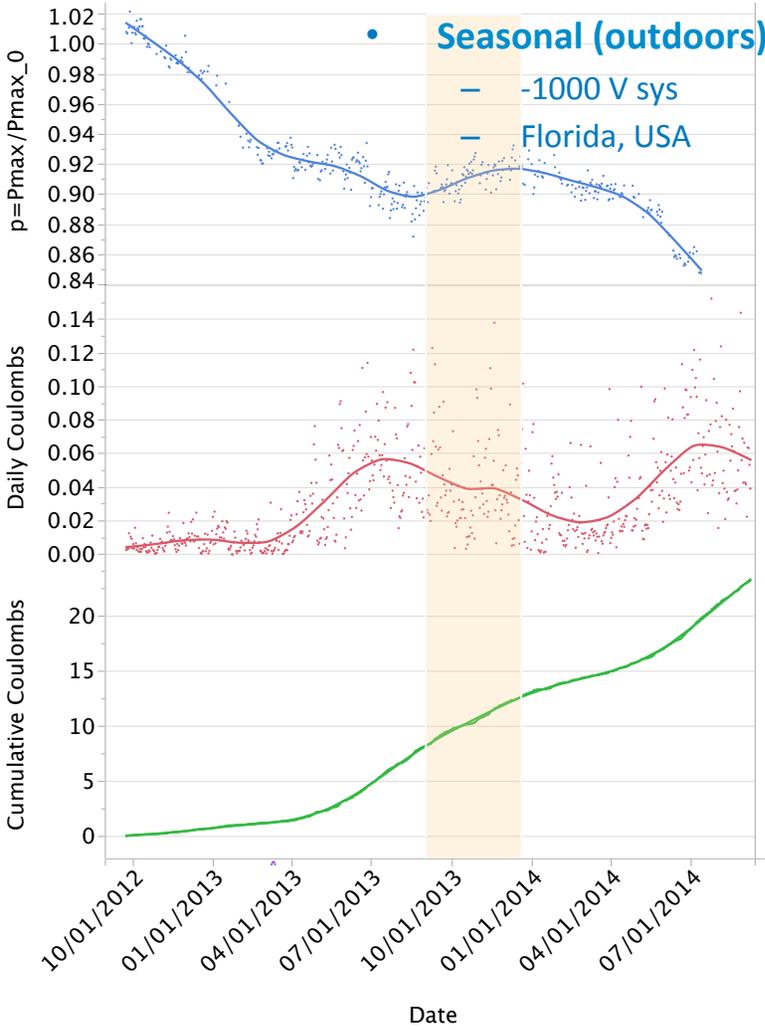
Mitigating Factor: previous PID stress history

- PID experience followed by recovery, can reduce sensitivity to further PID stress, or even lead to stability



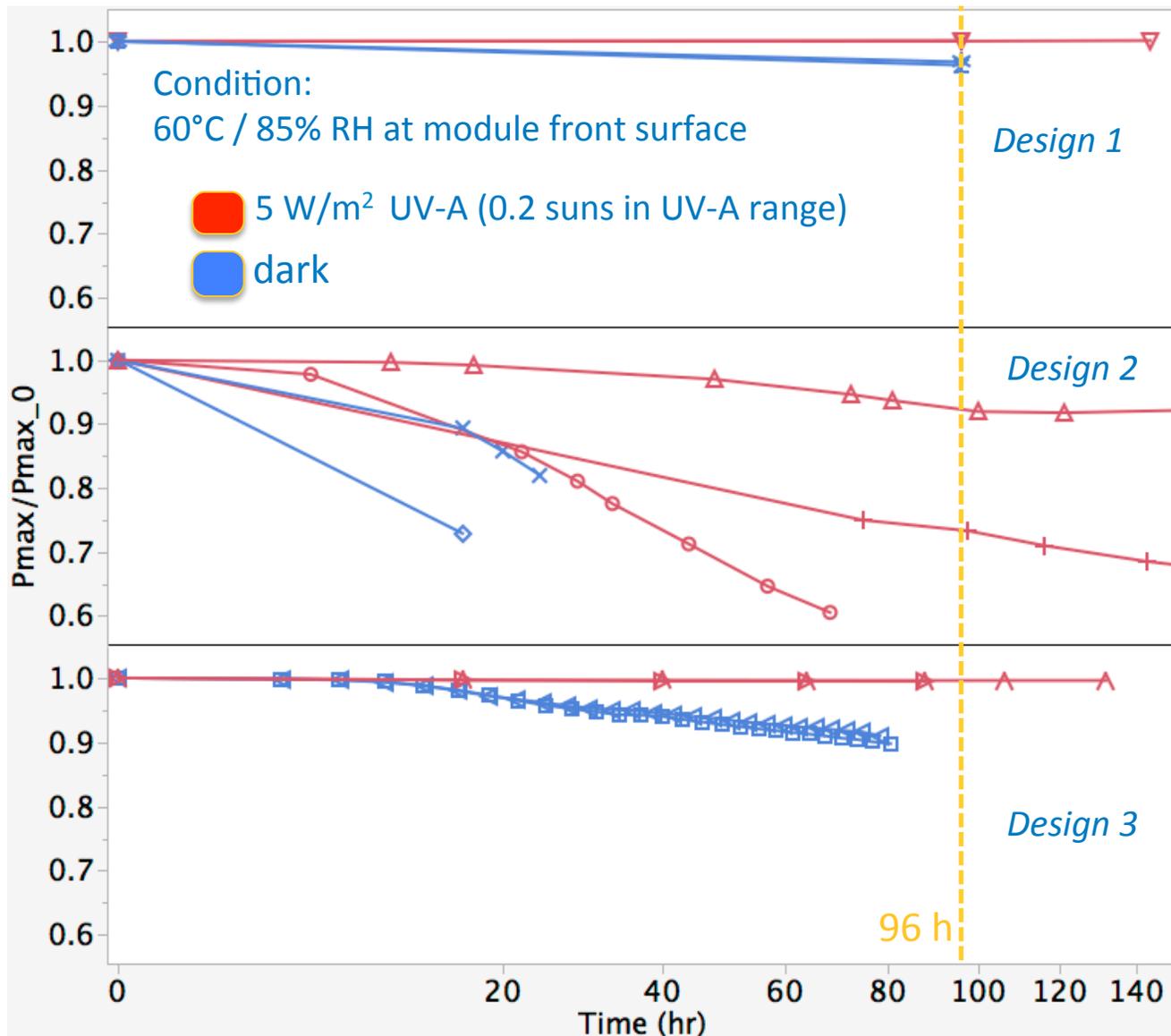
Hacke et. al, 37th IEEE PVSC (2011)

Mitigating Factor: Effective stress decrease



- Recovery seen with stress magnitude decrease

Mitigating Factor: Light

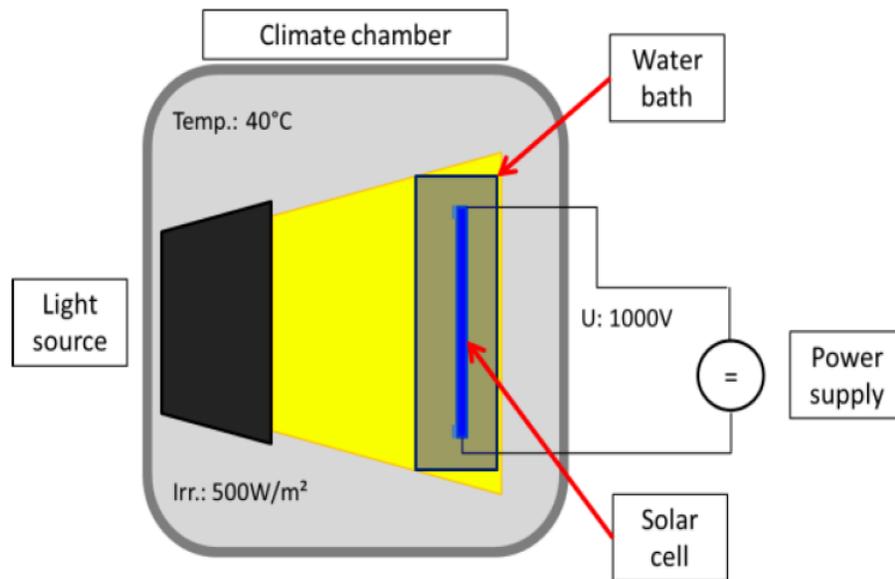


- T Chamber decreased and RH increased to maintain 60°C/85% RH on surface.
- Leakage current with UV at or above dark condition: leakage current not mitigated



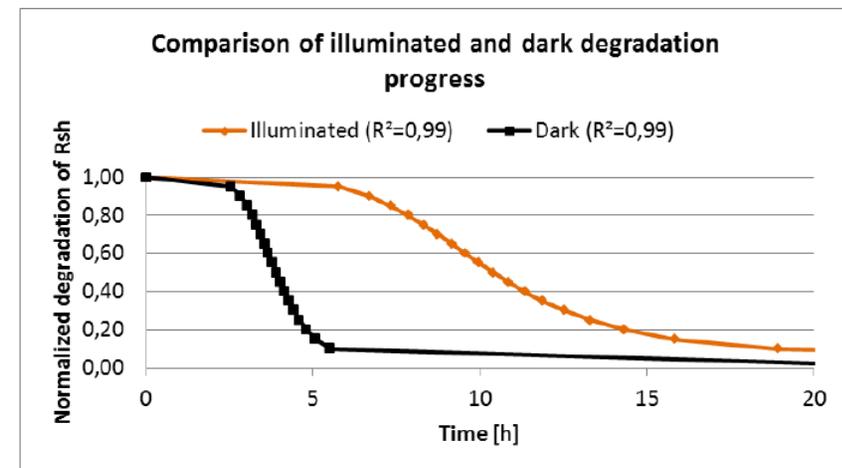
P. Hacke, 2014 NREL PV Module Reliability Workshop

Mitigating Factor: Light (continued)



- It seems that the degradation is slowed down by a higher SiN_x conductivity (further investigations have to be done)

- The PID is decelerated by irradiation
- The degradation phase is 2.4 times longer

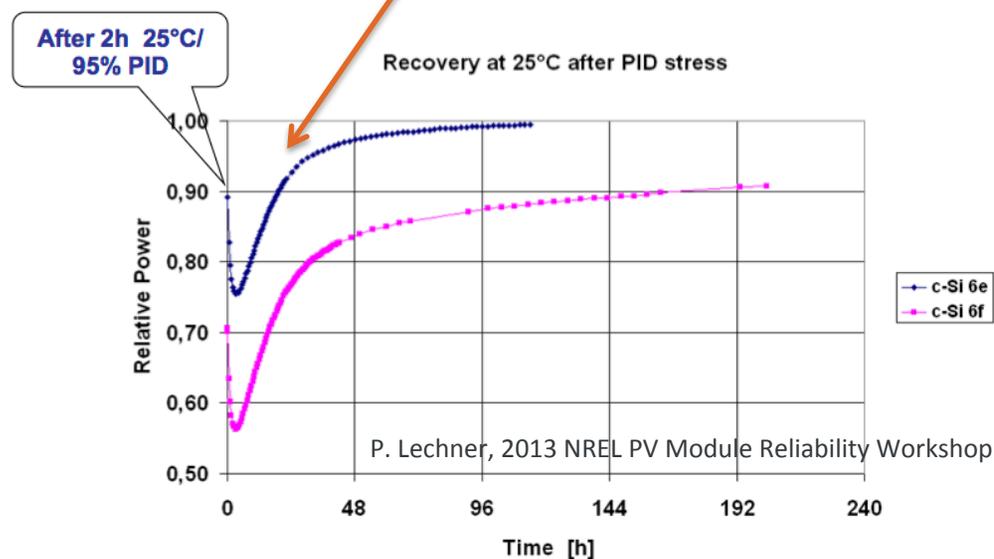
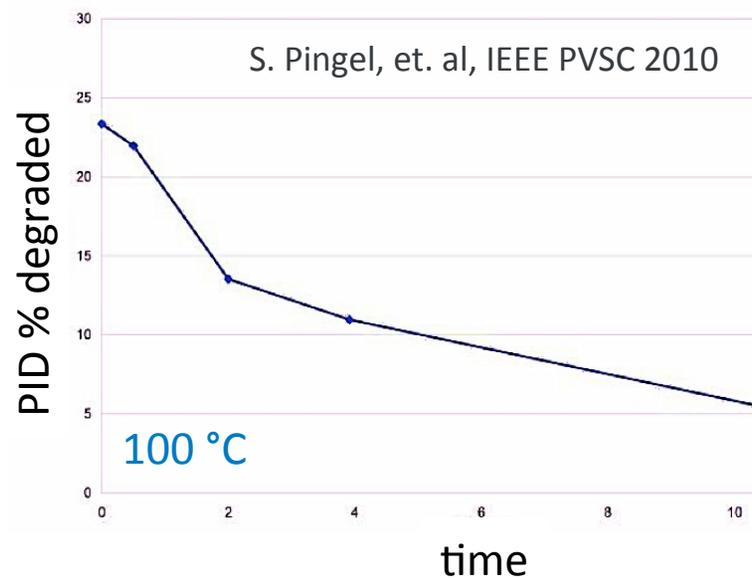


S. Koch, 2014 NREL PV Module Reliability Workshop

Mitigating factor: thermal activated recovery

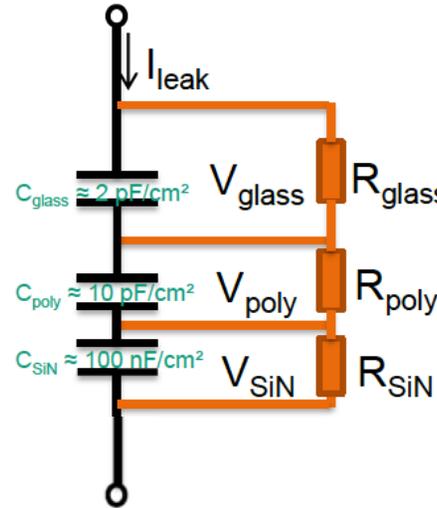
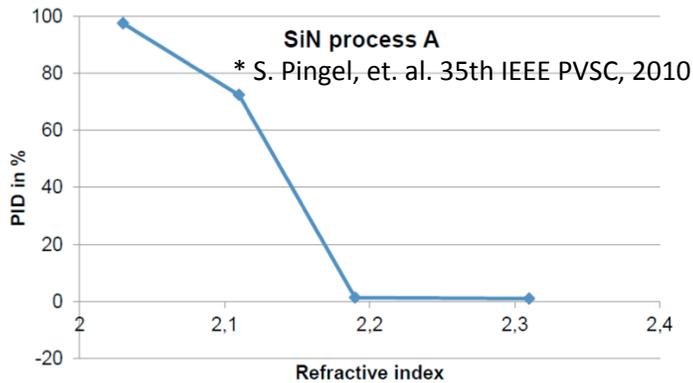
- **Removal or reduction of stress**
 - Drying of module
 - Removal of voltage potential (*ie, at night*)
- **Significant recover is frequently seen**
 - Out-diffusion of Na from stacking fault
 - Na in stacking fault apparently not energetically favorable
- **Much less recovery in extreme cases of degradation**

*PID Ionic charge motion
Electromotive (in EVA & SiN)
+
Diffusion (in oxide & silicon)*



- **Relevant recovery even at 25°C possible**
- **Acceleration at higher T**
- **E_a is 0.7 to 0.8 eV**

Factor: Charge build up over SiNx



SiN _x layer	refractive index	Si/N ratio	electronic conductivity	PID sensitivity
SiN1	1.93	low	low	high
SiN2	2.32	high	high	low

$$V_{SiN} = \frac{R_{SiN}}{R_{glass} + R_{poly} + R_{SiN}} V_{ext}$$

$$V_{SiN} = \frac{R_{SiN}}{R_{glass} + R_{poly} + R_{SiN}} V_{ext}$$

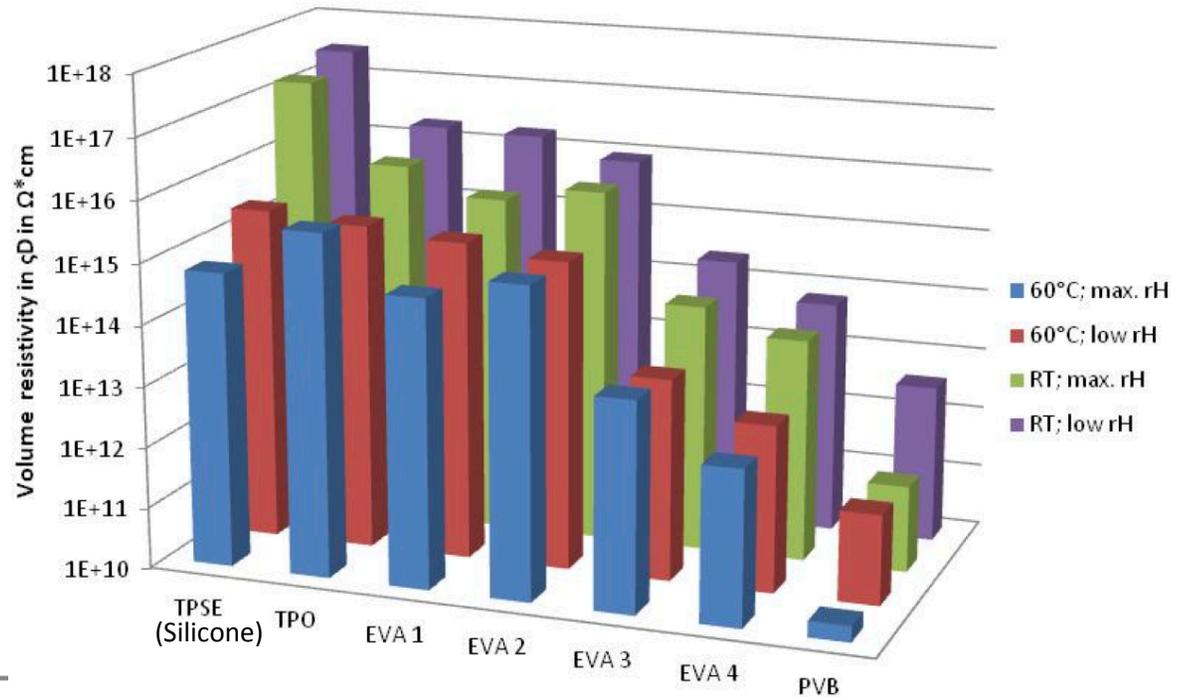
V. Naumann, 2014 NREL PV Module Reliability Workshop

- Index of SiNx refraction, closely linked to Si:Si bonding, SiNx conductivity, and ability to dissipate charge.
- Reducing voltage potential over SiNx (ie electromotive driving force for ions) can be achieved by decreasing R_{SiNx} or increasing $R_{glass} + R_{polymer}$

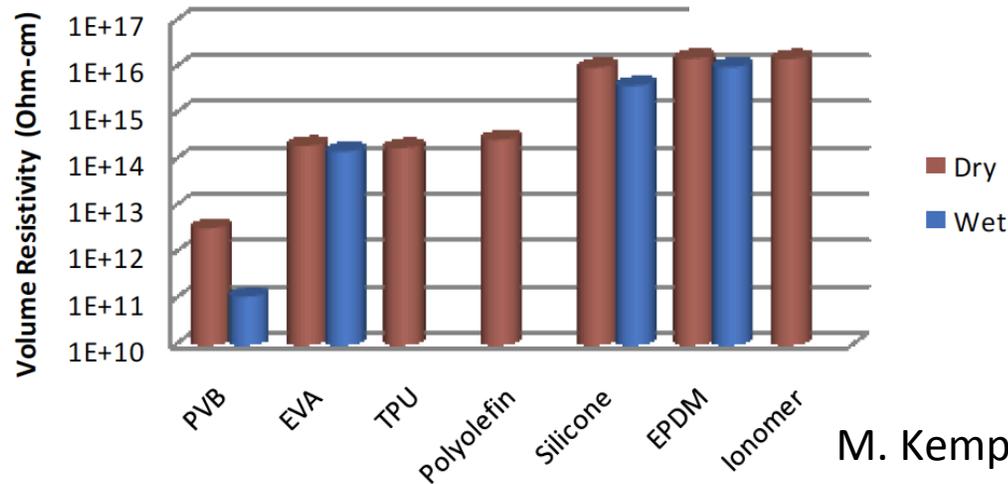
Factor: Encapsulant resistivity

- Ionic conductivity of encapsulants

- Temperature
- *Humidity Ingress*
- Quality (solute for mobile ions)
 - Impurities
 - Dangling bonds/polymerization



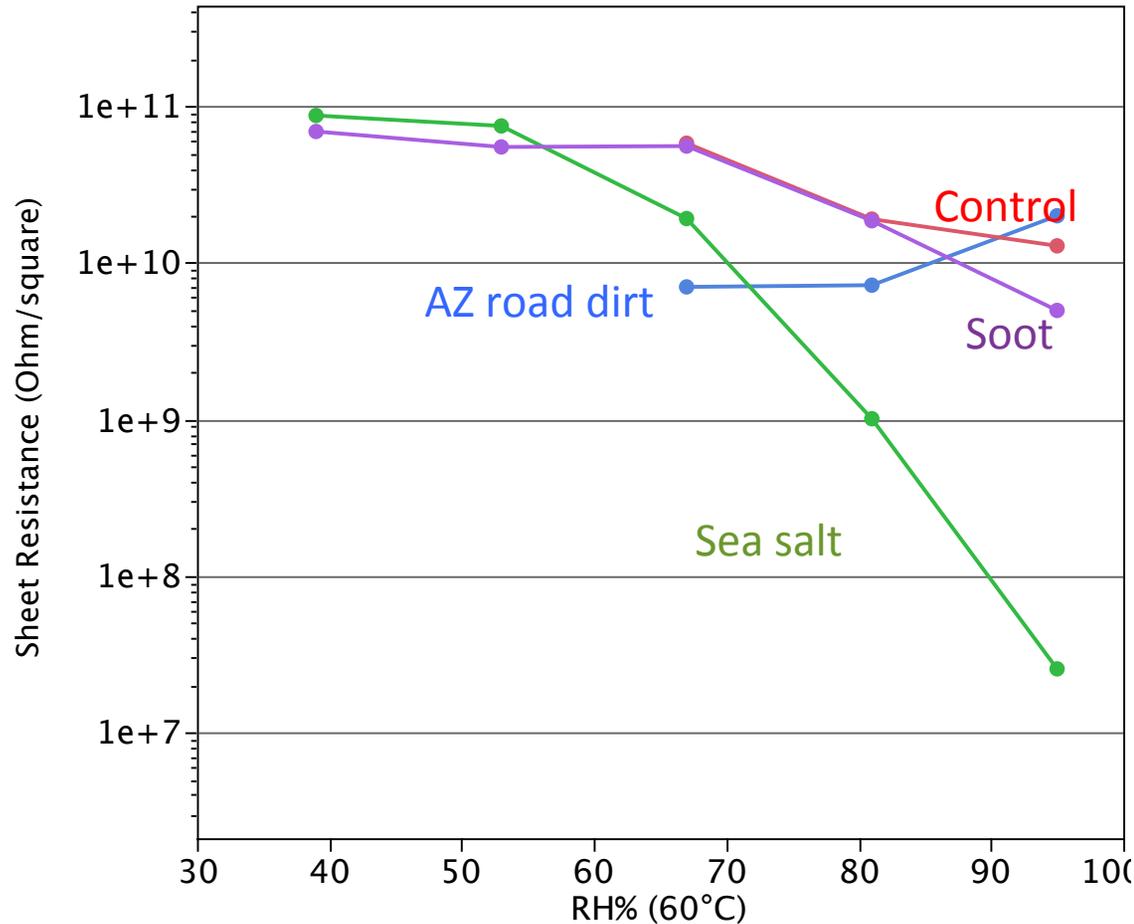
Berghold et. al IEEE PVSC (2014)



M. Kempe

Soiling

Sheet resistance as a function of soil type and relative humidity

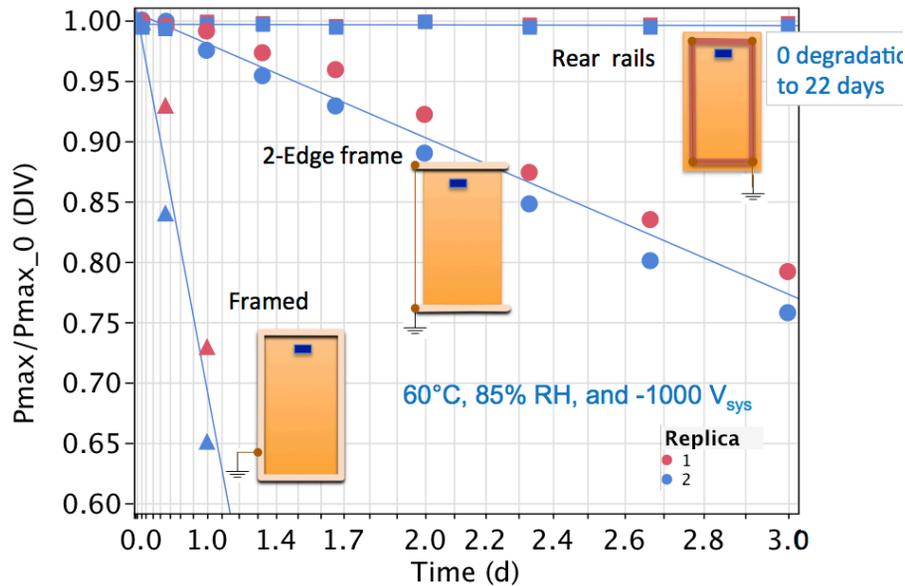


NREL-Hacke/Sandia-Burton,
Preliminary results
To be published

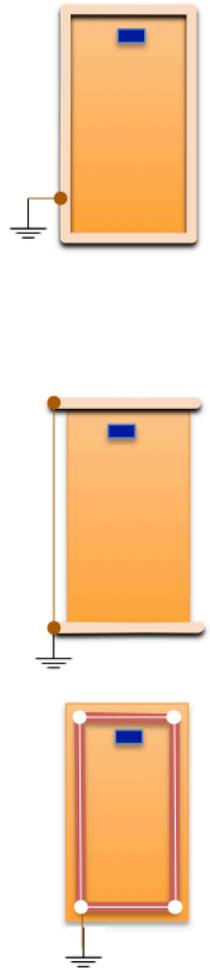
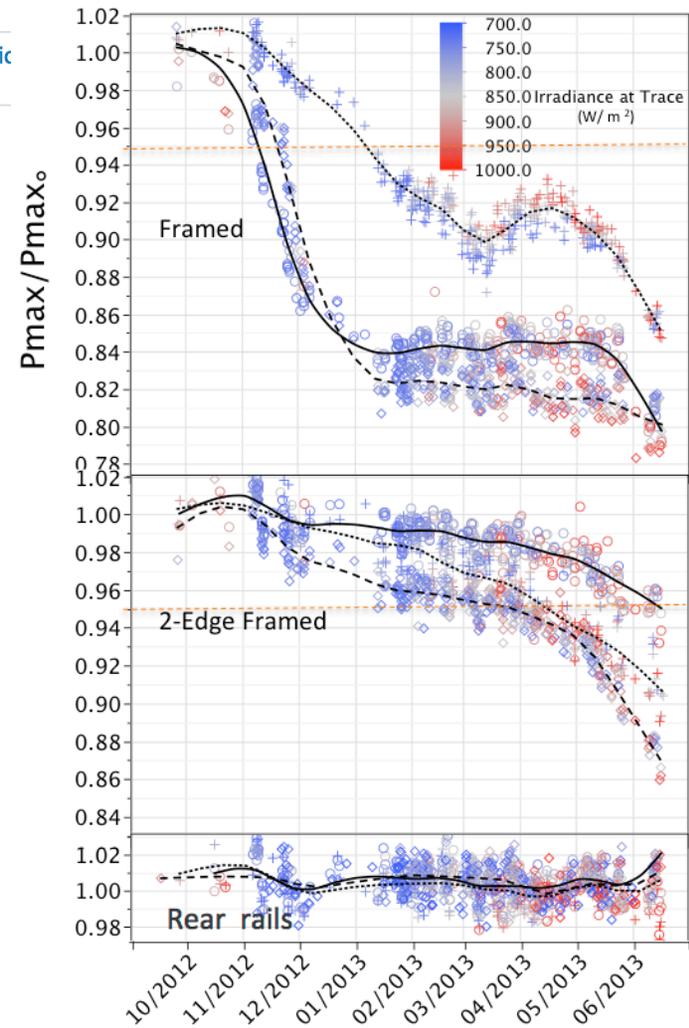
- Sea salt yields greatest decrease in glass surface face sheet resistance with RH
- AZ road dirt showed an important decrease, but less humidity dependence
- Decreased resistance over the glass face → higher conductivity to ground → accelerated PID

Mitigating Factor: Mounting

- Full metal frames vs. 2 edge frames vs. rear fiberglass rails



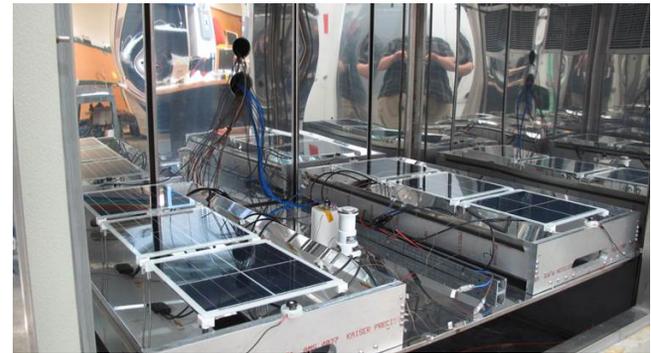
- Minimizing conduction to ground via framing mitigates PID
- Module dimensional effects can also matter
 - Distance from frame to active cell
 - Mounting angle
 - Grounded/ungrounded mounts



P. Hacke, et. al. 28 EU-PVSEC (2013)

Understanding of interactions

- Temperature
- Relative humidity
- Voltage
- PID Stress history/ effective stress
- Light
- Thermal-activated recovery
- Charge build-up over SiN
- Encapsulant resistivity
- Soiling
- Mounting
- ...



Combined and cyclic stress testing including multiple stress factors required for clarifying multiple, inter-related mechanisms

Future of IEC testing for system voltage stress

- **Test method development**
 - *c-Si exists in IEC 62804 TS ed.1*
- **Qualification testing (basic level)**
 - *Field experience*
 - *Validated modeling*
 - *Few factors (ie. T, RH, V)*
- **Climate-specific**
 - *Field experience*
 - *Validated modeling*
 - *Few factors (ie. T, RH, V, soil)*
- **Lifetime prediction**
 - *Combined/cyclic stress testing*
 - *Consideration of long term system voltage effects such as delamination, electrochemical corrosion.*

No hard walls between the categories above

To be integrated to some of the above:

Heterostructures
Thin film

Understanding of new technologies
Understanding of interactions

Thank you for your attention

The Alliance for Sustainable Energy, LLC (Alliance), is the manager and operator of the National Renewable Energy Laboratory (NREL). Employees of the Alliance, under Contract No. DE-AC36-08GO28308 with the U.S. Dept. of Energy, have authored this work. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a non-exclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for United States Government purposes.

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.